CLAIM AMENDMENTS

1. (previously amended)A transcoder, comprising:

an input that receives a first signal having a first signal type;

a transcoder functional block that transforms the first signal having the first signal type thereby generating a second signal having a second signal type, wherein the transcoder functional block includes:

a satellite receiver that is operative to decode the first signal having the first signal type;

a modulator, connected to an output of the satellite receiver, that is operative to modulate decoded output from the satellite receiver; and

a DAC (Digital to Analog Converter), connected to an output of the modulator, that is operative to transform the second signal having the second signal type from a digital signal into an analog signal;

an output that transmits the second signal having the second signal type;

wherein the first signal type includes a first modulation, a first code rate, a first symbol rate, and a first data rate; and

wherein the second signal type includes at least one of a second modulation, a second code rate, a second symbol rate, and a second data rate.

2. (original) The transcoder of claim 1, wherein:

the first signal type is a turbo coded signal that includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps.

3. (original) The transcoder of claim 1, wherein:

the first signal type is an LDPC (Low Density Parity Check) coded signal that includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol

rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30.5 Mbps.

4. (original) The transcoder of claim 1, wherein:

the transcoder functional block is implemented within an integrated circuit.

5. (previously amended)The transcoder of claim 4, wherein:

the transcoder functional block includes a first functional block and the second functional block; and

the first functional block and the second functional block are functional blocks within the integrated circuit.

6. (currently amended) The transcoder of claim 4, wherein:

the first functional block is ~~the~~ the satellite receiver that is operative to decode the first signal having the first signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog signal.

7. (previously amended)The transcoder of claim 4, wherein:

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operative to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operative to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operative to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog signal.

8. (original) The transcoder of claim 7, wherein:

the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.

9. (previously amended)The transcoder of claim 1, wherein:

the transcoder is implemented as at least one of a one to many transcoder, a uni-directional transcoder, and a bi-directional transcoder;

the one to many transcoder is operative to transform the first signal having the first signal type thereby generating the second signal having the second signal type and a third signal having the third signal type;

the uni-directional transcoder is operative to transform the first signal having the first signal type thereby generating the second signal having the second signal type when communicating in a first direction with respect to the transcoder;

the bi-directional transcoder is operative to transform the first signal having the first signal type thereby generating the second signal having the second signal type when information is communicated in a first direction with respect to the transcoder; and

the bi-directional transcoder is also operative to transform a fourth signal having a fourth signal type thereby generating a fifth signal having a fifth signal type when information is communicated in a second direction with respect to the transcoder.

10. (original) The transcoder of claim 1, wherein:

the transcoder is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cable television system, and a cable modem communication system.

11. (original) The transcoder of claim 1, wherein:

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that ensures that the second signal having the second signal type is a DVB STB (Set Top Box) compatible signal.

12. (previously amended)The transcoder of claim 1, wherein:

the transcoder functional block includes a first functional block and the second functional block;

a satellite signal, being a turbo coded signal and having an 8 PSK (Phase Shift Keying) modulation type, that is provided to a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner that is operative to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

the first functional block is an 8 PSK (Phase Shift Keying) turbo code receiver;

the analog baseband signal is provided to the 8 PSK turbo code receiver that is operative to decode the analog baseband signal thereby generating a decoded baseband signal;

the analog baseband signal is the first signal having the first signal type that is provided to the transcoder functional block;

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that is operative to transform the first signal having the first signal type thereby generating the second signal having the second signal type;

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operative to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

13. (previously amended)The transcoder of claim 12, further comprising:

a microcontroller or a state machine, connected to each of the satellite receiver and the modulator, that is operative to coordinate the communication and control of a Set Top Box (STB), to which the transcoder is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the transcoder is also communicatively coupled.

14. (original) The transcoder of claim 13, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

15. (original) The transcoder of claim 14, wherein:

each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

16. (previously amended)A transcoder, comprising:

an input that receives a first signal;

wherein the first signal includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second);

a transcoder functional block that transforms the first signal thereby generating a second signal, wherein the transcoder functional block includes:

a satellite receiver that is operative to decode the first signal;

a modulator, connected to an output of the satellite receiver, that is operative to modulate decoded output from the satellite receiver; and

a DAC (Digital to Analog Converter), connected to an output of the modulator, that is operative to transform the second signal from a digital signal into an analog signal;

an output that transmits the second signal; and

wherein the second signal includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps.

17. (original) The transcoder of claim 16, wherein:

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that ensures that the second signal having the second signal type is a DVB STB (Set Top Box) compatible signal.

18. (previously amended)The transcoder of claim 16, wherein:

the transcoder functional block includes a first functional block and the second functional block;

the first functional block includes a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner;

the transcoder functional block includes an 8 PSK (8 Phase Shift Key) turbo code receiver and a DVB (Digital Video Broadcasting) encoder/modulator;

the second functional block includes the DAC;

a satellite signal, being a turbo coded signal and having an 8 PSK modulation type, is provided to the CMOS satellite tuner that is operative to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

the analog baseband signal is the first signal;

the analog baseband signal is provided from the CMOS satellite tuner to the 8 PSK turbo code receiver that is operative to decode the analog baseband signal thereby generating a decoded baseband signal;

the DVB encoder/modulator receives the decoded baseband signal and generates a digital DVB signal;

the digital DVB signal is the second signal;

the DAC (Digital to Analog Converter) is operative to transform the second signal from the digital signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operative to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

19. (previously amended)The transcoder of claim 18, further comprising:

a microcontroller or a state machine, connected to each of the satellite receiver and the modulator, that is operative to coordinate the communication and control of a STB (Set Top Box), to which the transcoder is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the transcoder is also communicatively coupled.

20. (original) The transcoder of claim 19, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

21. (original) The transcoder of claim 20, wherein:

each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

22. (original) The transcoder of claim 16, wherein:

the first signal is a turbo coded signal.

23. (previously amended)A transcoder, comprising:

an input that receives a first signal;

wherein the first signal includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second);

a transcoder functional block that transforms the first signal thereby generating a second signal, wherein the transcoder functional block includes:

a satellite receiver that is operative to decode the first signal;

a modulator, connected to an output of the satellite receiver, that is operative to modulate decoded output from the satellite receiver; and

a DAC (Digital to Analog Converter), connected to an output of the modulator, that is operative to transform the second signal from a digital signal into an analog signal;

an output that transmits the second signal; and

wherein the second signal includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30.5 Mbps.

24. (original) The transcoder of claim 23, wherein:

the transcoder functional block includes a DVB (Digital Video Broadcasting) encoder/modulator that ensures that the second signal having the second signal type is a DVB STB (Set Top Box) compatible signal.

25. (previously amended)The transcoder of claim 23, wherein:

the transcoder functional block includes a first functional block and the second functional block;

the first functional block includes a CMOS (Complementary Metal Oxide Semiconductor) satellite tuner;

the transcoder functional block includes an 8 PSK (8 Phase Shift Key) LDPC (Low Density Parity Check) code receiver and a DVB (Digital Video Broadcasting) encoder/modulator;

the second functional block includes the DAC;

a satellite signal, being an LDPC coded signal and having an 8 PSK modulation type, is provided to the CMOS satellite tuner that is operative to perform tuning and down-converting of the satellite signal to generate an analog baseband signal having I, Q (In-phase, Quadrature) components;

the analog baseband signal is the first signal;

the analog baseband signal is provided from the CMOS satellite tuner to the 8 PSK LDPC code receiver that is operative to decode the analog baseband signal thereby generating a decoded baseband signal;

the DVB encoder/modulator receives the decoded baseband signal and generates a digital DVB signal;

the digital DVB signal is the second signal;

the DAC (Digital to Analog Converter) is operative to transform the second signal from a digital signal into an analog IF (Intermediate Frequency) signal;

an up-converter functional block that is operative to up-convert the analog IF signal to an L-band signal having a frequency in a range of 950 MHz to 2150 MHz; and

the L-band signal is a DVB STB (Set Top Box) compatible signal.

26. (previously amended)The transcoder of claim 25, further comprising:

a microcontroller or a state machined, connected to each of the satellite receiver and the modulator, that is operative to coordinate the communication and control of a STB (Set Top Box), to which the transcoder is communicatively coupled, and an LNB (Low Noise Block Converter) of a satellite dish to which the transcoder is also communicatively coupled.

27. (original) The transcoder of claim 26, further comprising:

a first transceiver that interfaces the microcontroller or a state machine to the LNB; and

a second transceiver that interfaces the microcontroller or a state machine to the STB.

28. (original) The transcoder of claim 27, wherein:

each of the first transceiver and the second transceiver is a DiSEqC (Digital Satellite Equipment Control) transceiver.

29. (original) The transcoder of claim 23, wherein:

the first signal is an LDPC coded signal.

30-67. (canceled)

68. (previously amended)A transcoding processing method, the method comprising:

receiving a first signal having a first signal type;

transcoding the first signal having the first signal type thereby generating a second signal having a second signal type, wherein the transcoding including;

employing a satellite receiver to decode the first signal having the first signal type;

employing a modulator, connected to an output of the satellite receiver, to modulate decoded output from the satellite receiver; and

employing a DAC (Digital to Analog Converter), connected to an output of the modulator, to transform the second signal having the second signal type from a digital signal into an analog signal;

outputting the second signal having the second signal type;

wherein the first signal type includes a first modulation, a first code rate, a first symbol rate, and a first data rate; and

wherein the second signal type includes at least one of a second modulation, a second code rate, a second symbol rate, and a second data rate.

69. (original) The method of claim 68, wherein:

the first signal type includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps.

70. (original) The method of claim 69, wherein:

the first signal is a turbo coded signal.

71. (original) The method of claim 68, wherein:

the first signal type is an LDPC (Low Density Parity Check) coded signal that includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second); and

the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30.5 Mbps.

72. (original) The method of claim 71, wherein:

the first signal is a turbo coded signal.

73. (previously amended)The method of claim 68, wherein:

the method is performed using a first functional block and a second functional block;

the first functional block includes the satellite receiver employed to decode the first signal having the first signal type; and

the second functional block includes ~~a~~ the modulator and the DAC employed to transform the second signal having the second signal type from the digital signal into the analog signal.

74. (previously amended)The method of claim 68, wherein:

the method is performed using a first functional block and a second functional block;

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operative to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operative to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operative to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog signal.

75. (original) The method of claim 74, wherein:

the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.

76. (previously amended)A transcoding processing method, the method comprising:

receiving a first signal having a first signal type;

wherein the first signal type includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 21.5 Msps (Mega-symbols per second), and a data rate of approximately 41 Mbps (Mega-bits per second)

transcoding the first signal having the first signal type thereby generating a second signal having a second signal type, wherein the transcoding including;

employing a satellite receiver to decode the first signal having the first signal type;

employing a modulator, connected to an output of the satellite receiver, to modulate decoded output from the satellite receiver; and

employing a DAC (Digital to Analog Converter), connected to an output of the modulator, to transform the second signal having the second signal type from a digital signal into an analog signal;

wherein the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 7/8, a symbol rate of approximately 20 Msps, and a data rate of approximately 32.25 Mbps;

outputting the second signal having the second signal type; and

wherein the first signal is a turbo coded signal.

77. (previously amended)The method of claim 76, wherein:

the method is performed using a first functional block and a second functional block;

the first functional block includes the satellite receiver employed to decode the first signal having the first signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog signal.

78. (previously amended)The method of claim 76, wherein:

the method is performed using a first functional block and a second functional block;

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operative to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operative to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operative to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog signal.

79. (original) The method of claim 78, wherein the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.

80. (previously amended)A transcoding processing method, the method comprising:

receiving a first signal having a first signal type;

wherein the first signal type includes an 8 PSK (Phase Shift Keying) modulation type, a code rate of 2/3, a symbol rate of approximately 20 Msps (Mega-symbols per second), and a data rate of approximately 40 Mbps (Mega-bits per second)

transcoding the first signal having the first signal type thereby generating a second signal having a second signal~~;~~ type, wherein the transcoding including;

employing a satellite receiver to decode the first signal having the first signal type;

employing a modulator, connected to an output of the satellite receiver, to modulate decoded output from the satellite receiver; and

employing a DAC (Digital to Analog Converter), connected to an output of the modulator, to transform the second signal having the second signal type from a digital signal into an analog signal;

wherein the second signal type includes a QPSK (Quadrature Phase Shift Keying) modulation type, a code rate of 6/7, a symbol rate of approximately 20 Msps, and a data rate of approximately 30. 5 Mbps;

outputting the second signal having the second signal type; and

wherein the first signal is an LDPC (Low Density Parity Check) coded signal.

81. (previously amended)The method of claim 80, wherein:

the method is performed using a first functional block and a second functional block;

the first functional block includes a satellite receiver that is operative to decode the first signal having the first signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog.

82. (previously amended)The method of claim 80, wherein:

the method is performed using a first functional block and a second functional block;

the first functional block includes a transport processor that includes a PID (Program Identification) filtering functional block, a PCR (Program Clock Reference) time stamp correction functional block, and a null packet insertion functional block;

the PID filtering functional block is operative to throw away data in the first signal having the first signal type;

the PCR time stamp correction functional block is operative to keep a time base of the first signal having the first signal type constant;

the null packet insertion functional block is operative to insert null packets into the second signal having the second signal type thereby ensuring a constant data rate of the second signal having the second signal type; and

the second functional block includes the modulator and the DAC that is operative to transform the second signal having the second signal type from the digital signal into the analog signal.

83. (original) The method of claim 82, wherein the transport processor is an MPEG-2 (Motion Picture Expert Group, level 2) transport processor.